What is claimed is:

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1. A method for programming a field mounted device having a memory, the method comprising the steps of:

running a computational process having data read access to an activated first memory area storing a programmable first device configuration;

deactivating the first memory area, wherein said step comprises precluding said computational process to access the first memory area; and

activating a deactivated second memory area storing a programmable second device configuration, wherein said step comprises granting said computational process data read access to the second memory area.

2. The method of claim 1, further comprising the steps of:

running a first configuration process having data read and write access to the deactivated second memory area; and

storing data in the second memory area for modifying the second device configuration in the second memory area.

3. The method of claim 2, further comprising the step of

executing the first device configuration in the first memory area by the computational process during running the first configuration process.

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4. The method of claim 2, further comprising the steps of:

running a second configuration process having data read and write access to a deactivated third memory area; and

storing data in the third memory area.

5. The method of claim 3, further comprising the steps of:

precluding the second configuration process access to the second memory area by granting the first configuration process an exclusive access to the second memory area;

modifying via said second configuration process the second device configuration in the second memory area; and

granting the computational process access to the second memory area after said modifying step.

6. The method of claim 2, further comprising the step of

storing the first device configuration into the second memory area.

7. The method of claim 1, further comprising the steps of:

writing over a first branch address that references the first memory area with a second branch address that references the second memory area for deactivating the first memory area and activating the second memory area in a single write access.

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8. The method of claim 7, further comprising the steps of:

deactivating the first memory area upon the occurrence of a hardware or software error in the first memory area; and

activating the second memory area upon said occurrence of said error.

9. The method of claim 7, further comprising the step of

copying the first device configuration from the first memory area into the second memory area.

10. The method of claim 9, further comprising the step of

executing the first device configuration in the first memory area by the computational process during the copying step.

11. A programmable field mounted device, comprising:

a memory circuit including a plurality of memory areas, each memory area storing program codes, each memory area selectively activated;

a control circuit configured to generate a selection signal, the selection signal activating one of the plurality of memory areas to create an activated memory area containing a first programm code representing a first device configuration, and deactivating the one of the remaining memory areas to create a deactivated memory area for storing a second programm code representing a second device configuration.

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12. The device of claim 11, wherein the control circuit includes a microprocessor, the microprocessor having read access to the activated memory area for excuting the first programm code.

13. The device of claim 11, further comprising a configuration device configured to modify the second program code in the deactivated memory area.

14. The device of claim 13, wherein the control circuit is configured to grant the configuration device read and write access to the deactivated memory area for modifying the second programm code.

15. The device of claim 11, wherein the control circuit is further configured to deactivate the activated memory area containing the first program code and activate the deactivated memory area containing the modified second program code.

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~~16. The device of claim 12 and 15, wherein the control~~ circuit is further configured to provide the microprocessor read access to the memory area containing the second ~~programm code for executing said program code.~~

17. The device of claim 11, wherein the deactivated memory area containing the second programm code is activated by

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writing in the memory circuit a branch address corresponding to said memory area.

18. The device of claim 11, wherein the activated memory area containing the first programm code is deactivated by writing over a branch address in the memory circuit corresponding to said memory area address with the branch address corresponding to the memory area containing the second programm code.

19. The device of claim 11, wherein the memory circuit is a non-volatile memory.

20. The device of claim 11, wherein the memory circuit is an EEPROM.

21. The device of claim 11, further including an energy storage device configured to store energy for at least one write access to the memory circuit.

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22. A method for programming a field mounted device running a computational process, the method comprising the steps of:

activating a first memory area storing a first programmable configuration;

deactivating a second memory area storing a second programmable configuration;

configuring the second memory area with a modification of the second programmable configuration; and

coordinating the configuration of the second memory area with the computational process, the coordination of the configuration of the second memory area including the steps of simultaneously executing the first programmable configuration in the first memory area by the computational process during configuration of the second memory area with a modification of the second programmable configuration, deactivating the first memory area storing the first programmable configuration upon completion of configuring the second memory area with a modification of the second programmable configuration, and activating the second memory area upon completion of configuring the second memory area with a modification of the second programmable configuration.

23. The method of claim 22, wherein the step of

activating the second memory area and deactivating the first memory area comprises the step of writing over a first branch address that references the first memory with a second branch address that references the second memory area.

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24. The method of claim 22, wherein the step of coordinating the configuration of the second memory area with the computational process further comprises the steps of:

precluding the computational process access to the second memory area;

granting a configuration process exclusive access to the second memory area; and

granting the computation process access to the second memory area after the modifying step.

25. The method of claim 22, wherein the step of activating the second memory area and deactivating the first memory area is accomplished by a single write access to a branch address.

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